Reg. No. : | | | | | | | | | | |

H 0720

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2011

THIRD SEMESTER

ELECTRONICS AND COMMUNICATION ENGINEERING

EC1201 DIGITAL ELECTRONICS

(REGULATION 2008)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State shannons expansion theorem.

2. Realize OR gate using NAND gates only.

3. List out the merits of totem pole configuration.

4. Compare TTL and CMOS logic families.

5. Write down the truth table of a 4 to 2 encoder.

6. Draw the logic diagram of a half subtractor circuit.

7. Convert a JK flipflop to D flip flop.

8. Draw the timing diagram for a mod-4 asynchronous up counter.

9. Distinguish between static RAM and dynamic RAM.

10. What is the size of the decoder in a 32 × 10 ROM?

PART B — (5 × 16 = 80 marks)

11. Use tabulation method to obtain the minimal SOP format

$F = \Sigma m(6, 7, 8, 9)\ fd\ (10, 11, 12, 13, 14, 15)$.

Or

12. Realize a Z-input XOR gate using NAND gates only and NOR gates only.

13. Draw and explain the working of ECL OR/NOR gate.

Or

14. Draw and explain the working of a two input CMOS NAND and NOR gates.

15. (a) Design a 4 bit parallel binary adder/subtractor using full adders. (8)

(b) Write short notes on data selector and data distributor. (8)

Or

16. (a) Realize 4 to 16 decoder using two 3 to 8 decoder. (8)

(b) Implement $F = \Sigma m(1, 3, 4, 11, 12, 13, 14, 15)$ using an 8 × 1 multiplexer. (8)

17. Draw and explain the working of a 4 bit Johnson counter with a neat timing diagram.

Or

18. (a) Design a mod-3 asynchronous up counter using JK flipflops. (6)

(b) Explain in detail about fundamental mode and pulse mode asynchronous circuits. (10)

19. (a) Design a full adder using a suitable PROM. (8)

(b) Write short notes on PAL. (8)

Or

20. Briefly explain about FPGA with a neat block diagram.

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